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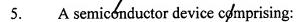
## What is claimed:

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1 A	comicondi	intor device	comprising
1. A	SCHILCOHU	ctor device	COMPRISING

- a protective insulation layer;
- a pad opening section provided in the protective insulation layer;
- a wiring layer which the pad opening section reaches; and
- a wiring layer provided at a level lower than the wiring layer which the pad opening section reaches.

wherein the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

- 2. A semiconductor device according to claim 1, wherein the wiring layer which the pad opening section reaches is composed of one layer.
- 3. A semiconductor device according to claim 1, wherein the wiring layer which the pad opening section reaches is composed of two layers.
  - 4. A semiconductor device according to faim 1, wherein the wiring layer which the pad opening section reaches has a thickness that is greater than that of the wiring layer provided at a level lower than the wiring layer which the pad opening section reaches.



a first wiring layer formed above a semiconductor layer through a first interlayer insulation layer;

a second wiring layer that provides a pad section formed above the first wiring layer through a second interlayer insulation layer;

a protective insulation layer formed above the second wiring layer and the second interlayer insulation layer; and

a pad opening section provided in the protective insulation layer,

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wherein an upper surface of the first interlayer insulation layer includes a first region where the protective insulation layer is formed vertically thereabove, and the first wiring layer is formed on the first region.

- 6. A semiconductor device according to claim 5, wherein
- the upper surface of the first interlayer insulation layer further comprises a second region where the pad opening section is formed vertically thereabove, and at least part of the second interlayer insulation layer is formed on the second region.
  - 7. A semiconductor device according to claim 5, wherein the first wiring layer includes a plurality of wiring layers in the same layer, and the plurality of wiring layers are formed on the first region.
  - 8. A method for manufacturing a semiconductor device, the method comprising the steps of:
    - (a) forming a wiring layer on an interlayer insulation layer;
  - (b) forming a protective insulation layer on the interlayer insulation layer and the wiring layer; and
  - (c) forming a pad opening section in the protective insulation layer, which reaches the wiring layer,

wherein the semiconductor device includes a wiring layer provided at a level lower than the wiring layer to which the pad opening section reaches,

wherein the pad opening section is formed such that the wiring layer provided at a level lower than the wiring layer to which the pad opening section reaches is formed outside a region of the pad opening section as viewed in a plan view.

9. A method for manufacturing a semiconductor device according to claim 8, wherein the wiring layer which the pad opening section reaches is composed of one layer.

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1	10. A method for manufacturing a semiconductor device according to claim 8,		
2	wherein the wiring layer which the pad opening section reaches is composed of two layers.		
1	11. A method for manufacturing a semiconductor device according to claim 8,		
2	wherein the wiring layer which the pad opening section reaches has a thickness that is		
3	greater than that of the wiring layer provided at a level lower than the wiring layer which the		
4	pad opening section reaches.		
1	12. A semiconductor device according to claim 5, wherein the first wiring layer	r	
2	is only formed on the first region.		
1	13. A semiconductor device according to claim 6, wherein the first wiring layer	r	
2	is only formed on the first region and the second interlayer insulating layer is formed over		
3	the entire second region.		
1	14. A semiconductor device as in claim 13, wherein a portion of the second		
2	interlayer insulating layer is formed over the first region.		
1	15. A semiconductor device as in claim 5, further comprising:		
2	a third wiring layer positioned between the first wiring layer and the second wiring		
3	layer; and		
4	a third interlayer insulation layer positioned between the first interlayer insulation		
5	layer and the second interlayer insulation layer.		
1	16. A semiconductor device as in claim 15, wherein the third wiring layer is		



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17. A method for manufacturing a semiconductor device, comprising:

forming a lower level wiring layer;

forming an lower level interlayer dielectric layer on and adjacent to the lower level wiring layer;

forming an upper level wiring layer above the lower level interlayer dielectric layer, wherein the lower level wiring layer is electrically connected to the upper level wiring layer;

forming a protective insulation layer on the upper level wiring layer;

removing a first portion of the protective insulation layer over the upper level wiring layer and over the lower level interlayer dielectric layer to form a pad opening section of the upper level wiring layer,

wherein a second portion of the protective insulation layer located vertically above the lower level wiring layer remains after removing the first portion of the protective layer; and

wherein no portion of the lower level wiring layer is disposed vertically below the pad opening section.

- 18. A method as in claim 17, further comprising forming an intermediate wiring layer and an intermediate interlayer dielectric layer; wherein the intermediate wiring layer is positioned above the lower level wiring layer and below the upper level wiring layer; and the intermediate interlayer dielectric layer is positioned above the lower level interlayer dielectric layer and below the upper level wiring layer.
- 19. A method as in claim 18, wherein no portion of the intermediate lower level wiring layer is disposed vertically below the pad opening section.

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1	20. A method as in claim 18, further comprising:
2	forming the lower level wiring layer to be electrically connected to the intermediate
3	level wiring layer;
4	forming the intermediate level wiring layer to be electrically connected to the upper
5	level wiring layer;
6	forming the lower level wring layer to include has a thickness that is less than that
7	of the lower level interlayer dielectric layer;
8	forming the intermediate level wiring layer to include a thickness that is less than
9	that of the intermediate level interlayer dielectric layer;
10	forming a plurality of lower level plugs to electrically connect the lower level wiring
11	layer to the intermediate/level wiring layer;
12	forming a plurality of intermediate level plugs to electrically connect the
13	intermediate level wiring layer to the upper level wiring layer; and
14	wherein the intermediate plugs are formed to be offset from the lower level
15	intermediate plugs in a vertical direction.

- A method as in taim 17, further comprising forming a reflection prevention 21. film on the upper level wiring layer.
- A method as in claim 21, further comprising removing the reflection 22. prevention film from the pad opening section of the upper level wiring layer.
- A device as in claim 5, further comprising a reflection prevention film 1 formed on the second wining layer. 2

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